Scaling of a-InGaZnO TFTs and Pixel Electrode for AM-LCDs

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The channel length (L) and width (W) scaling behavior of amorphous In-Ga-Zn-O thin-film transistors (TFTs) have been investigated. The fabricated TFTs have a mobility of ~12 cm^2/V-s, sub-threshold slope (S) of ~110 mV/decade, threshold voltage around 0.3 V and off-current below 10^{-13} A. Even though the TFTs with smaller channel length ($L \leq 5$ μm) show proper switching characteristics, threshold voltage lowering and sub-threshold slope degradation are observed, while off-current and mobility are not changed. The mobility degradation with L, which was observed in amorphous silicon TFTs, is not seen for short channel a-IGZO TFTs. Lastly, the necessity of the TFT scaling for a pixel electrode in AM-LCD applications is discussed.

1. Introduction

Due to the higher mobility (> 10 cm^2/V-s), steeper sub-threshold swing (< 200 mV/decade), and long-range uniformity, an amorphous In-Ga-Zn-O (a-IGZO) Thin-Film Transistor (TFT) has received considerable attention in the field of active matrix liquid crystal display (AM-LCD) applications. Achieving higher pixel density (> 300 pixels per inch, PPI) is one of future technology trends in the area of the "retina-like" AM-LCD.[14] It is important to notice that the TFT miniaturization (channel width (W) and length (L) scaling) is a critical limitation for high resolution displays. Also the performance of TFTs is directly influenced by geometrical factors, such as W and L.

In this paper, we present an in-depth study of the scaling dependency of coplanar homojunction a-IGZO TFTs. The coplanar homojunction a-IGZO TFTs investigated in this paper utilize a hydrogen doped a-IGZO source/drain (S/D) region to achieve a low resistance S/D contacts. It was previously reported that this structure has the advantages of good ohmic S/D contact, small parasitic capacitance, and the capability of achieving a small channel length.[1]

2. Experimental

Coplanar Homojunction TFT Structure

Fig. 1 shows schematic cross-section of the fabricated coplanar homojunction a-IGZO TFT. The Mo layer (100 nm) was sputtered on a glass substrate as the gate electrode. PECVD was used to deposit the a-SiO_x gate insulator (200 nm). The a-IGZO film (30 nm) was D.C. sputtered and defined using a diluted hydrochloric acid. A 150 nm a-SiO_x channel protection layer (CPL) was R.F. sputtered and patterned by dry etching. The CPL defines the TFT's width and length. The CPL patterning was followed by a PECVD of amorphous hydrogen rich silicon nitride (a-SiN_x:H) to passivize the TFTs. During this PECVD process, hydrogen in the reactive chamber and/or in the a-SiN_x:H layer dopes the exposed a-IGZO region and increases its electrical conductivity, so the hydrogen doped a-IGZO region works as a source/drain. More experimental details about the fabrication process can be found in the reference (1).

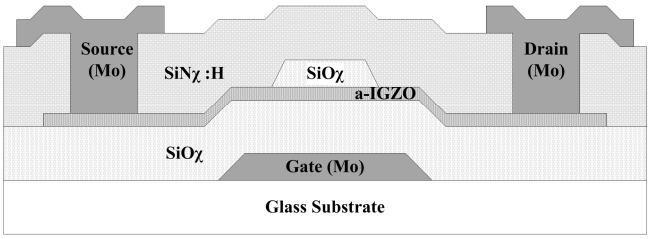

Fig. 1. Cross-sectional schematic of the fabricated coplanar homojunction a-IGZO TFT.

Measurements

All measurements were carried in an electrically shielded dark box using the Agilent 4156C semiconductor parameter analyzer. The ideal MOSFET I_D–V_{GS} equations are used to extract the device parameters in linear and saturation regimes.[2]

$$I_D = \mu C_G \frac{W}{L}\left(V_{GS} - V_{TH}\right)\cdot V_{DS} \quad \text{(linear regime)} \quad (1)$$

$$I_D = \mu C_G \frac{W}{2L}\left(V_{GS} - V_{TH}\right)^2 \quad \text{(saturation regime)} \quad (2)$$

where C_G is the gate capacitance per unit area. The V_{TH} is the

threshold voltage, and V_{DS} and V_{GS} are drain-to-source and gate-to-source voltage, respectively. The sub-threshold swing (S) is defined as $S \equiv (\partial logI_D/\partial V_{GS})^{-1}$ at around a maximum $(\partial logI_D/\partial V_{GS})^{-1}$ point. The leakage current, I_{OFF}, is defined as I_D when $V_{GS} = -10V$. The above equations are manually programed in MATLAB software and used for extracting all TFT's parameters. The TFTs, from uniformly distributed six dies over a same substrate, are selected for measurement samples. The average value and standard deviation of the extracted parameters are used for the following discussion.

3. Results and Discussion

Channel Length Dependency

To study a channel length dependency of TFTs, transfer curves (I_D-V_{GS}) with various L (from 3 – 120 μm) are compared in Fig. 2. The W is fixed at 60 μm. From Fig. 2, we conclude that all TFTs demonstrate normal TFT operation and the TFT's I_D is increasing as L is decreasing. This observation is in good agreement with the ideal MOSFET equations.

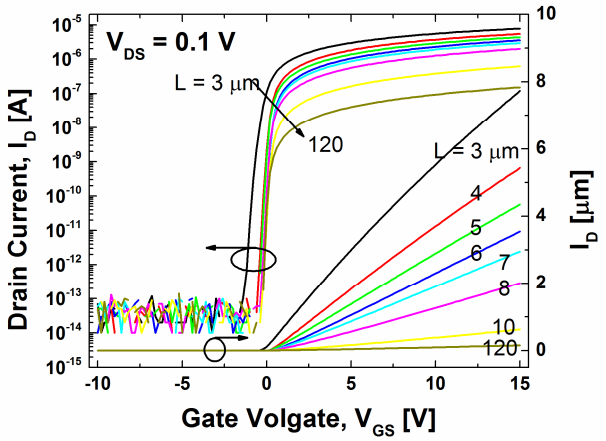

Fig. 2. Transfer characteristics (I_D-V_{GS}) of the coplanar homojunction a-IGZO TFTs with various channel length, L.

The key parameters of TFTs are summarized as a function of L in Fig. 3. With shorter L, the V_{TH} decreases and S increases (i.e. less steep). These changes become more severe when the TFT's L is smaller than 5 μm. Furthermore, we should note that TFTs with large L (L ≥ 5 μm) work in the enhancement mode ($V_{TH} > 0$ V) while TFTs with small L (L < 5 μm) work in the depletion mode ($V_{TH} < 0$V). The enhancement mode TFTs are more suitable for circuit design because the depletion mode TFTs result in a high leakage current and produces distorted waveforms in integrated circuits.[3)]

The change on V_{TH} can be understood by a charge sharing model and a drain induced potential barrier lowering (DIBL) effect in short channel MOSFETs.[4,5)] The changes in V_{TH} and S have been easily observed in short channel MOSFETs which are not scaled properly. The channel charges (electrons) near the source/drain (S/D) are controlled by the electric field originating not only from the gate, but also from the S/D electrodes (charge sharing). In short channel TFTs, the portion of channel charges, which is exclusively controlled by the gate electrode, reduces; the portion of the charges, which is shared by the gate and S/D electrodes, increases. Hence, less gate voltage is required to control the channel charges, so resulting the V_{TH} lowering. Therefore, it takes a lower gate voltage to reach the threshold condition.

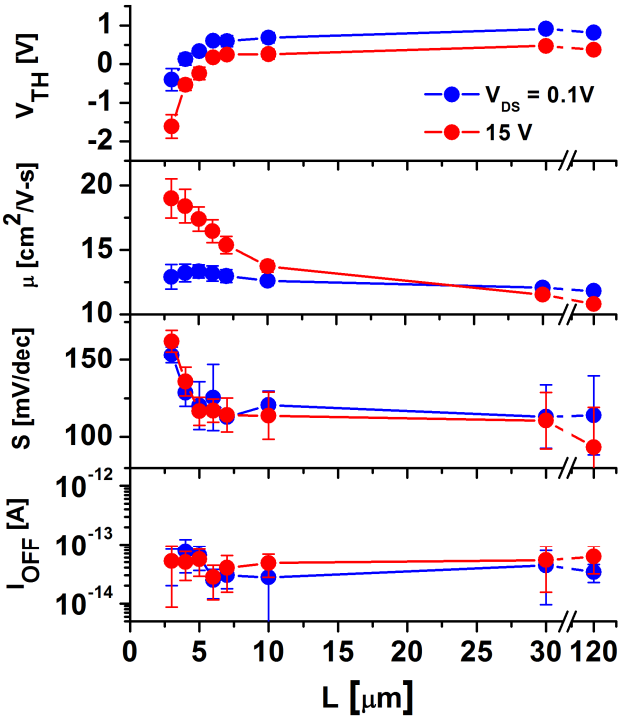

Fig. 3. Channel length dependency of V_{TH}, μ, S and I_{OFF}, (filled dots: average value, bars: standard variation)

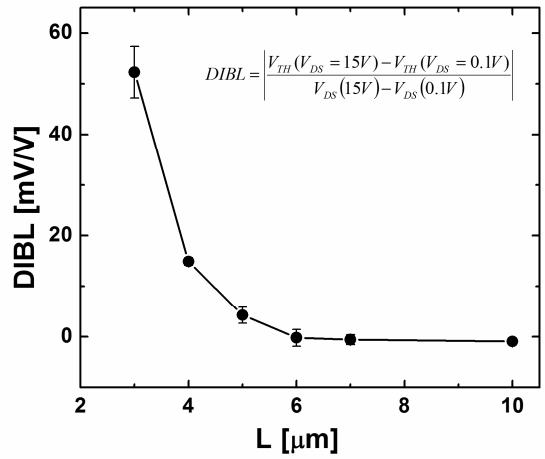

Fig. 4. Evolution of DIBL coefficient along with L (filled dots: average value, bars: standard variation)

Alternatively, the drain voltage in a short channel FET would help the gate voltage to accumulate the electron in the channel. In other words, the drain voltage induces the lowering of the source-to-channel potential barrier and V_{TH} is decreased as V_{DS} increases. This phenomenon is named as a drain-induced barrier-lowering (DIBL) and the DIBL coefficient is defined by eq. (3). The increase of DIBL in short L TFTs are shown in Fig. 4.

$$DIBL = \left| \frac{V_{TH}(V_{DS} = 15V) - V_{TH}(V_{DS} = 0.1V)}{V_{DS}(15V) - V_{DS}(0.1V)} \right| \quad (3)$$

Considering the changes in the sub-threshold swing, the thermionic emission current across the energy barrier is increased because of the barrier being lowered, resulting in degradation of S. We believe that these explanations can also be applied to a-IGZO TFTs. Lastly, the I_{OFF} of a-IGZO TFTs does not change for smaller channel length, while the I_{OFF} increases linearly with L in hydrogenated amorphous silicon (a-Si:H) TFTs.[6] This is attributed to the low hole-density in a-IGZO material.

Furthermore, we investigate the mobility changes for different channel lengths. The mobility of a-IGZO TFTs is almost constant in linear region. However, the saturation region mobility increases with decrease of TFT channel length. This is due to the reduction of the effective channel length (L_{eff}) by increasing the shrinkage of the channel length, ΔL, at higher V_{DS}. (L_{eff}=L-ΔL) When L is small, the difference between L_{eff} and L is significant and the extracted mobility is increased accordingly.

It is worthy to compare the mobility dependency with that of a-Si:H TFTs. For short channel a-Si:H TFTs, a decrease in mobility with small channel length ($L \leq 10$ μm) has been observed in both linear and saturation regimes[7,8] This effect is caused by the increased magnitude of the source/drain resistance in comparison to channel resistance for short channel a-Si TFTs. However, in coplanar homojunction a-IGZO TFTs, the mobility degradation is not observed until L = 3 μm. The measured contact resistance of coplanar homojunction a-IGZO TFTs is about 33 Ω·cm, which is about two orders of magnitude reduced value from that of a-Si:H TFTs. The R_{SD}·W of a-Si:H TFTs is typically about 2~10 kΩ·cm.[8-10] Furthermore, this contact resistance is even smaller than the values from previously reported a-IGZO TFTs.[11,12] Therefore, we conclude that a coplanar homujuction a-IGZO TFT has the advantage over the channel length scaling.

Lastly, the output characteristics have been investigated. The output curves for the TFT (L=3 and 120 μm) are shown in Fig. 5. The inset of the figure shows details for 0 V ≤ V_{DS} ≤ 1 V; no current crowding is found near the origin in both Ls, implying that the S/D contact is good ohmic with small R_{SD}. The r_{out} is defined by the following equation in the device saturation region and the extracted r_{out} for various L are illustrated in Fig. 6.

$$r_{out}^{-1}(V_{GS}) = \left. \frac{\partial I_D}{\partial V_{DS}} \right|_{V_{GS}} \quad \text{(saturation regime)} \quad (3)$$

It is observed that the r_{out}^{-1} dramatically increases for L ≤ 5 μm; the output resistance r_{out} rapidly decreases for L ≤ 5 μm. The r_{out} can be de-emphasized for the TFT purpose of a simple switch. In contrast, for the purpose of TFT amplifiers or inverters, the r_{out} should be considered as an important design parameter. It is known that a smaller r_{out} results in a smaller gain in the amplifier.

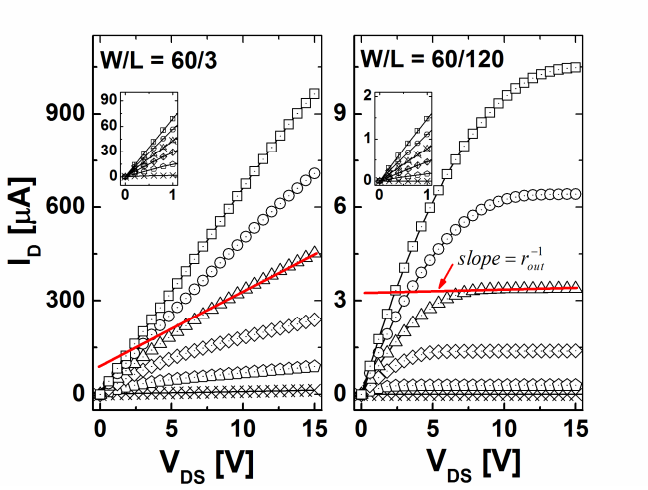

Fig. 5. Output curves of the fabricated TFTs with L = 3 and 120 μm, (inset) details for 0 ≤ V_{DS} ≤ 1 V, (red line) slope for the calculation of output resistance

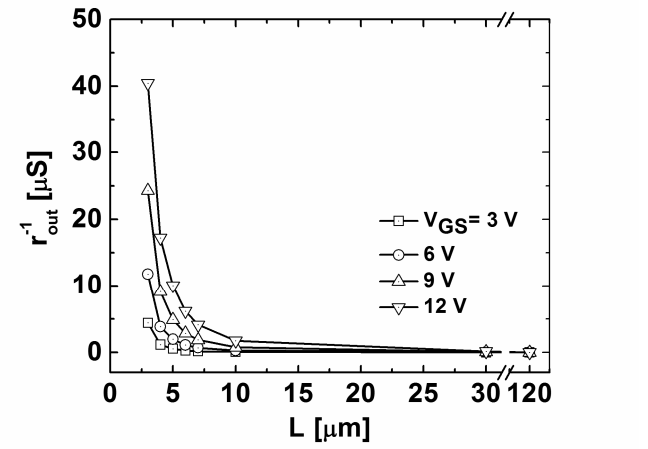

Fig. 6. The dependency of output resistance (r_{out}) on various L

Channel Width Dependency

Similar analysis is done for various W (from 10 μm ≤ W ≤ 120 μm). L is fixed at 10 μm. Although the channel width is varied from 1x to 12x of the channel width, we do not observe noticeable changes on the TFT parameters. Thus, the channel width is not a serious consideration because the channel width which is larger than the length is usually adapted in applications.

TFT scaling and pixel aperture ratio

From eq. (1-2), it is concluded that the scaling of L can increase the current if the mobility is not degraded. Furthermore, even if it is not required to have the larger current, the TFT's W can also be decreased with the reduced L. The down-scaling of W and L is closely related with the pixel aperture ratio (AR). AR is defined by the ratio between the area of pixel electrode which is transparent and total pixel area. Hence, smaller TFT has an advantage to achieve a higher AR for a given pixel area. By shrinking the TFT's size, it is possible to extend the pixel electrode are, resulting in increased AR[13] Fig. 7a shows the increase of AR with reduction of TFT area for the AM-LCD pixel. On the other hands, if the allowed pixel area is decreased (higher PPI) without the scaling of TFT, a reduction of AR is unavoidable. To prevent the decrease of AR, the TFT size must be scaled down. (Fig. 7b)

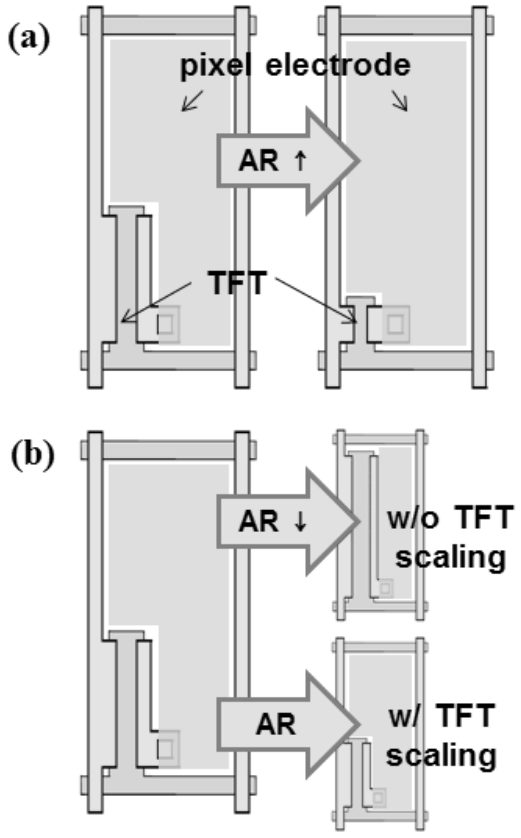

Fig. 7. (a) AR increases by the scaling of TFT for the given pixel area (b) AR is maintained by the scaling of TFT for the reduced pixel area

4. Conclusions

We have studied the channel width/length dependency of coplanar homojunction a-IGZO TFTs with 200 nm thick PECVD a−SiO_x. The mobility degradation along with the channel length, which was a disadvantage of a-Si:H TFTs, is not observed for short channel a-IGZO TFTs. The fabricated TFTs have a proper TFT operation and show good ohmic contact with small R_{SD}. However, in the case of TFTs with $L \leq 5$ μm, r_{out} and S degrade rapidly and negative V_{TH} is observed. We did not observe any noticeable W dependency on the TFTs. Even though there are degradations of V_{TH}, S and r_{out}, the fabricated a-IGZO TFTs with smaller channel length ($L \leq 5$ μm) show proper switching characteristics for AM-LCD applications. The scaling of a-IGZO TFTs will help to design the pixel electrodes for maintaining/enhancing the aperture ratio of high resolution AM-LCD.

Acknowledgments

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